



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kamel Benaissa, et al.

Docket No: TI-30681

Serial No: 09/994,421

Conf. No: 9408

Examiner: Edward J. Wojciechowicz

Art Unit: 2815

Filed: 11/27/2001

For: SEMICONDUCTOR VARACTOR WITH REDUCED PARASITIC RESISTANCE

2815
4/Election
P. Wulth
1-21-03

ELECTION

Assistant Commissioner for Patents
Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on 1-16-03.

Ann Trent
Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed December 17, 2002.

Applicants hereby elect to pursue Group II of Claims 1-5, 11-14, and 19-22, drawn to method of making a semiconductor device, without traversing the Examiner's restriction requirement.

Respectfully submitted,

Peter K. McLarty
Peter K. McLarty
Attorney for Applicants
Reg. No. 44,923

Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-4258

RECEIVED
JAN 17 2003
TECHNOLOGY CENTER 2800